IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit	: 2816	**Customer No. 26794**
Examiner	: Kenneth B. Wells	
Serial No.	: 10/648,022	
Filed	: August 26, 2003	
Inventor	: Christopher N. Brindle	Docket No.: 17987 [TYC-02-1522R]
Title	: SERIES/SHUNT SWITCH : AND METHOD OF CONTROL	Confirmation No.: 3501 Dated: January 30, 2007

Pre-Appeal Brief Request for Review

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicant respectfully requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reasons stated on the following pages.

Claims 1, 2, 6-11, 13-15, 18, and 19 stand rejected as allegedly being obvious over Sasabata in view of Kawai. In the Amendment dated September 22, 2006, the Applicants discussed the statements of the Examiner describing the disclosures of Sasabata and Kawai, which appear in paragraph 4 of the Official Action dated October 31, 2006, and paragraph 3 of the Official Action dated June 20, 2006. In that Amendment, the Applicants argued that the Examiner mischaracterized the features of Sasabata and Kawai as being equivalent to the features recited in the instant application, and that the Examiner failed to provide a factual basis for such a characterization. (see the arguments presented on pgs. 8 and 10 of the Sept. 22, 2006 Amendment). Specifically, the Applicants argued that the semi-conductor 52 of Kawai (which includes two transmission gates 61, 62, each formed by a CMOS), is not equivalent to the single shunt FET recited in the claims. (see pg. 10, first paragraph of the Sept. 22, 2006 Amendment). In addition, the Applicants requested an Affidavit of Official Notice under 37 C.F.R. 1.104(d)(2) regarding the Examiner's characterization, which request was not acknowledged. (Id.)

The Applicants also argued that even if, *arguendo*, the Examiner were correct in his characterization, that the theoretical combination of Sasabata and Kawai would still fail to recite all of the features recited in the claims. (see the arguments presented on pg. 8, second full paragraph of the Sept. 22, 2006 Amendment). That is, that applying a voltage source to one of two CMOS transmission gates 61, 62 in a semi-conductor switch 52 (Kawai) does not enable one of the transmission gates 61, 62 to be turned ON while simultaneously turning OFF a series FET (connected to the switch 52), and vise versa. (Id.)

The Applicants further argued that the Examiner failed to provide a proper motivation for combining Sasabata and Kawai, and that citing as motivation "...to obtain the well-known

advantages associated with such a transmission gate structure..." fails to qualify as actual evidence of motivation, as required under *In re Dembiczak*, 50 USPQ2d 1614, 1616-17 (Fed. Cir. 1999). (see the arguments presented on pg. 10, first full paragraph, and pg. 11, last paragraph of the September 22, 2006 Amendment).

In the latest Official Action, dated October 31, 2006, the Examiner raised a new rejection. Claims 1, 2, 6-11, 13-15, 18, and 19 were rejected as allegedly being indefinite for misdescribing that a control voltage applied to a common node of two FETs may be continuously applied thereto. (see paragraph 2 of the Official Action dated Oct. 31, 2006). The Examiner is again mischaracterizing the claim features of the instant application. The *continuous* limitation clearly refers to the coupling relationship between the voltage source and the common node of two FETs. For reasons unknown to the Applicants, the Examiner is asserting that the claims recite a single logic level providing both a high and low logic level. It is noted that the Applicants make no recitation or reference whatsoever to the "logic level" of the control voltage. Indeed, the Applicants recite that a control voltage (whether it be at a high or low logic level) be continuously coupled to a common node of two FETs, and that what ever its level, this continuous control voltage may simultaneously turn one FET ON and the other FET OFF.

The Applicants therefore respectfully request review of the obviousness and indefinite rejections of Claims 1, 2, 6-11, 13-15, 18, and 19.

Respectfully Submitted,

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